IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:				
Shunpei Yamazaki et al.)))			
Serial No.: 09/848,642))			
Filed: May 3, 2001				
Examiner: Andrew Schechter				
Art Unit: 2871				
For: Electro-Optical Device With Light Shielding Portion Comprising Laminated Colored Layers, Electrical Equipment Having The Same, Portable Telephone Having The Same)))))			
Confirmation No.: 2871				

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

TRANSMITTAL OF ENGLISH TRANSLATION OF PRIORITY DOCUMENT

In furtherance of Amendment H filed April 5, 2007, in response to the Office Action of January 25, 2007, Applicants are submitting herewith a verified English translation of the priority document Japanese patent application serial number 2000-140960 filed May 12, 2000 in Japan. A certified copy of this priority Japanese application was filed May 3, 2001 with the filing of this U.S. application.

Therefore, as explained in Amendment H, <u>Yamazaki</u> (US 7,023,021) is <u>not</u> prior art to the present application.

In particular, the present application claims priority under 35 USC §119 of Japanese

patent application serial number 2000-140960 filed May 12, 2000 in Japan. A certified copy

and translation of this priority Japanese application have now been filed.

Hence, as the §119 priority filing date of the present application is prior to the U.S. filing

date of Yamazaki (February 2, 2001), Yamazaki '369 is not prior art to the present application.

Accordingly, it is respectfully requested that Yamazaki be withdrawn as prior art to the

present application.

Conclusion

Therefore, for the reasons discussed in Amendment H, the present application is

allowable over the prior art, is in a condition for allowance and should be allowed.

Applicant does not believe that an extension of time is necessary for this submission.

However, if such an extension of time is needed, please consider this a petition for such an

extension of time and please charge our deposit account 50/1039 for the fee for such an

extension.

If any further fee is due for this submission, please charge our deposit account 50/1039.

Favorable consideration is earnestly solicited.

Date: June 11, 2007

Respectfully submitted,

/Mark J. Murphy/

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Shunpe	ei Yamazaki et al.)
Serial I	No.: 09/848,642) Art Unit: 2871
Filed: I	May 3, 2001) Examiner: Andrew Schechter
For:	Electro-Optical Device With Light Shielding)
	Portion Comprising Laminated Colored)
	Layers, Electrical Equipment Having The)
	Same, Portable Telephone Having The Same)

VERIFICATION OF TRANSLATION

Commissioner for Patents P.O.Box 1450 Alexandria, VA 22313-1450

Dear Sir:

I, Keiko Yamazaki, C/O Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached English translation of the Japanese Patent Application No. 2000-140960 filed on May 12, 2000; and

that to the best of my knowledge and belief the following is a true and correct English translation of the Japanese Patent Application No. 2000-140960 filed on May 12, 2000.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 7th day of June, 2007

Name: Keiko Yamazaki

[Name of Document] Patent Application [Reference Number] P004893 [Filing Date] May 12, 2000 [Attention] Commissioner, Patent Office, Takahiko KONDO [International Patent Classification] H01L 21/00 [Inventor] [Address] 398, Hase, Atsugi-shi, Kanagawa-ken c/o Semiconductor Energy Laboratory Co., Ltd. [Name] Shunpei YAMAZAKI [Inventor] [Address] 398, Hase, Atsugi-shi, Kanagawa-ken c/o Semiconductor Energy Laboratory Co., Ltd. [Name] Yuugo GOTO [Inventor] [Address] 398, Hase, Atsugi-shi, Kanagawa-ken c/o Semiconductor Energy Laboratory Co., Ltd. [Name] Hideki KATSURA

[Applicant]

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[Identification Number] 000153878

20 [Name] Semiconductor Energy Laboratory Co., Ltd.

[Representative] Shunpei YAMAZAKI

[Indication of Handlings]

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[List of Attachment]

[Attachment] Specification 1

[Attachment] Drawing 1

[Attachment] Abstract 1

[Document Name]

Specification

[Title of the Invention] ELECTRO-OPTICAL DEVICE

[Scope of Claims]

[Claim 1]

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An electro-optical device characterized by comprising:

a TFT; and

a light shielding portion formed of a stacked layer of a first colored layer and a second colored layer,

the light shielding portion is formed overlapping with at least a channel forming region of the TFT.

[Claim 2]

An electro-optical device characterized by comprising:

a plurality of pixel electrodes; and

a light shielding portion formed of a stacked layer of a first colored layer and a 15 second colored layer,

the light shielding portion is formed overlapping with a gap between any pixel electrode and a pixel electrode that is adjacent to the pixel electrode.

[Claim 3]

The electro-optical device according to any one of claims 1 and 2, characterized in that the first colored layer is blue.

[Claim 4]

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The electro-optical device according to any one of claims 1 and 2, characterized in that the second colored layer is red.

[Claim 5]

The electro-optical device according to any one of claims1 to 4, characterized in that the light shielding portion is provided over a substrate where a switching elements is formed.

[Claim 6]

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The electro-optical device according to any one of claims 1 to 4, characterized in that the light shielding portion is provided over an opposing substrate.

[Claim 7]

The electro-optical device according to any one of claims 1 to 6, characterized in that the electro-optical device is a transmission type liquid crystal display device in which the pixel electrode is formed of a transparent conductive film.

[Claim 8]

The electro-optical device according to any one of claims 1 to 7, characterized in that the electro-optical device is a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, or an optical game machine.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The invention of this specification relates to a semiconductor device having a circuit constructed of a thin film transistor (hereinafter referred to as TFT), and to a method of manufacturing the same. For example, the invention relates to an electro-optical device, which is represented by a liquid crystal display panel, and to electronic equipment loaded with the electro-optical device as a part.

[0002]

Note that, in this specification, the semiconductor device refers to general devices which can function by utilizing semiconductor characteristics, and the electro-optical devices, semiconductor circuits and the electronic equipment are all semiconductor devices.

5 [0003]

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[Prior Art]

In recent years, an attention has been paid on a technique for constructing a thin film transistor (hereinafter referred to as TFT) using a semiconductor thin film (on the order of several ~ several hundred nm in thickness) formed over a substrate having an insulating surface. The TFTs are widely used for electronic devices such as an IC or an electro-optical device, and the development thereof as a switching element for a liquid crystal display device in particular is in urgent need.

[0004]

In the liquid crystal devices, an active matrix liquid crystal display device in which, to obtain an image with high quality, pixel electrodes are arranged in the form of matrix and the TFT is used as a switching element connected to the respective pixel electrodes is attracting attention.

[0005]

The active matrix liquid crystal display devices are roughly classified into two known kinds of types that are a transmission type and a reflection type.

[0006]

The transmission type liquid crystal display device emits light from the back of a liquid crystal using a backlight and adjusts the passage of light by making use of a birefringence property and an optical activity of the liquid crystal to conduct display.

Further, the transmission type liquid crystal display device is further increasing in demand as a displaying display for a mobile computer or a video camera.

[0007]

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Further, in the liquid crystal display device, the TFTs having semiconductors made of amorphous silicon or polysilicon, are arranged in the form of matrix, and a liquid crystal material is sandwiched between an active matrix substrate where pixel electrodes, source lines and gate lines each connected to the TFTs are formed, and an opposing substrate having an opposing electrode arranged oppositely thereto. Besides, a color filter for displaying colors is stuck on the opposing substrate. And polarization plates are arranged over the active matrix substrate and the opposing substrate respectively, as optical shutters, to display color images.

[8000]

This color filter has colored layers of R (red), G (green), and B (blue), and a light shielding mask for covering only gaps between pixels, and light of a red color, a green color and a blue color is extracted by transmittance of the light through the color filter. The light shielding mask is for showing the screen clearly. This light shielding mask is generally constructed of a metallic film (chromium etc.) or an organic film containing a black pigment. This color filter is formed at a position corresponding to the pixel, thereby being capable of changing the color of the light to be extracted for each pixel. Note that, the position corresponding to the pixel means the position that accords with the pixel electrode.

[0009]

[Problems to be Solved by the Invention]

In a conventional liquid crystal display device using a metallic film as a light

shielding mask of a color filter, there has been a problem in that a parasitic capacitance with other wirings is formed and delay in signals tends to occur. Further, in consideration of the environment, an attention is paid on a non-chromium material. Furthermore, in the case that an organic film containing a black pigment is used as a light shielding mask of a color filter, a problem of an increase in manufacturing steps has occurred.

[0010]

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[Means for Solving the Problem]

The present invention is characterized by a pixel structure shielding a gap between TFTs and pixels from light without using a light shielding mask (black matrix). The present invention has a feature in that, as one of light shielding means, a stacked film of two colored layers (a stacked film of a red-colored layer and a blue-colored layer) is formed over an opposing substrate as a light shielding portion so as to overlap with a TFT on an element substrate.

15 [0011]

In this specification, a "red-colored layer" absorbs a part of the light emitted onto the colored layer to extract red-color light. Further, similarly, a "blue-colored layer" absorbs a part of the light emitted onto the colored layer to extract blue-color light, and a "green colored" absorbs a part of the light emitted onto the colored layer to extract green-color light.

[0012]

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A structure of the invention disclosed in this specification is an electro-optical device which is characterized by including a TFT, and a light shielding portion formed of a stack of a first colored layer and a second colored layer, in which the light shielding

portion is formed overlapping with at least a channel forming region of the TFT.

[0013]

Further, another structure of the invention is an electro-optical device which is characterized by including a plurality of pixel electrodes, and a light shielding portion formed of a stack of a first colored layer and a second colored layer, in which the light shielding portion is formed overlapping with a gap between any pixel electrode and a pixel electrode that is adjacent to the pixel electrode.

[0014]

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Moreover, in each of the above structures, the first colored layer is characterized by being blue. Further, the second colored layer is red.

[0015]

The electro-optical device is characterized in that the light shielding portion described above is provided over a substrate where a switching element is formed.

[0016]

Further, in each of the above structures, the light shielding portion described above is provided over an opposing substrate.

[0017]

Furthermore, in each of the above structures, the electro-optical device described above is the electro-optical device characterized by being a transmission type liquid crystal display device in which the pixel electrode is made of a transparent conductive film.

[0018]

[Embodiment Mode of the Invention]

An embodiment mode of the invention of this specification is described below.

[0019]

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The structure of the present invention is shown in Fig. 1. Here, a transmission type liquid crystal display device is taken as an example and is described below.

[0020]

Fig. 1(A) shows an example of appropriately forming colored layers $11 \sim 13$ of three colors, and of structuring a light shielding portion 15 and pixel openings $17 \sim 19$. In general, the colored layer is formed using a color resist made of an organic photosensitive material with a pigment dispersed.

[0021]

The light shielding portion 15 is formed so as to shield a gap between respective pixels from light. Accordingly, incident light is absorbed by the light shielding portion 15 and recognized to be mostly black by an observer. Further, the light shielding portion 15 is formed so as to overlap with a pixel TFT on an element substrate, and serves to shield the pixel TFT from outside light.

15 [0022]

The light shielding portion 15 is formed stacking the blue colored layer 11 and the red colored layer 12. The blue colored layer is simultaneously patterned into the colored layer (B) 11 and the light shielding portion 15 (R+B). Further, the red colored layer is simultaneously patterned into the colored layer (R) 12 and the light shielding portion 15 (R+B).

[0023]

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It is noted that Fig. 1(B) shows a sectional structure where the light shielding portion and the pixel openings in Fig. 1(A) are cut along the chain line (A1-A1'). Fig. 1(B) is an example in which after the colored layer (G) 13 is formed over an opposing

substrate 10, by stacking the colored layer (B) 11 and the colored layer (R) 12, the light shielding portion 15 (R+B), the pixel opening (B) 17, the pixel opening (R) 18 and the pixel opening (G) 19 are formed. Thus, in Fig. 1(C), after the colored layer (B) 11 is formed over the opposing substrate 10, the colored layer (R) 12 is formed. Further, the colored layers are covered by a leveling film 14.

[0024]

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Besides, with respect to the stacked film (the light shielding portion 15) of the blue colored layer (B) 11 and the red colored layer (R) 12, the respective transmittivities are measured under certain measurement conditions (white light source (D65), viewing angle: 2°, objective lens: 5 times). Measurement results are shown in Table 1.

[Table 1]

Transmittivity in the two-layer stacked layer of the colored layer

wavelength	transmittivity (color resist for transmitting)			
[nm]	R+B	G+B	R+G	
400	6.6%	14.7%	7.6%	
450	3.2%	7.7%	1.8%	
500	3.4%	23.4%	2.5%	
550	0.6%	6.1%	3.8%	
600	0.4%	0.5%	15.4%	
650	1.1%	0.5%	2.1%	
700	2.4%	1.1%	12.9%	
750	1.2%	1.5%	24.9%	
800	36.2%	30.7%	56.0%	

5 Measurement conditions: D light source Viewing angle: 2 Objective lens ×5 [0026]

Further, Table 1 is graphed in Fig. 3.

[0027]

As shown in Table 1 and Fig. 3, the transmittivity of the R+B (corresponding to the light shielding portion 15) becomes 7% or less in the visible light region (in a wavelength region of 400 ~ 700 nm), and the R+B sufficiently functions as a light shielding mask.

[0028]

Further, if three layers of colored layers are stacked, although a light shielding property is enhanced, since the unevenness thereof is enlarged in accordance with the three stacked layers, the flatness of the substrate is eliminated, and therefore, disturbance occurs in a liquid crystal layer. In particular, this is a major problem to a liquid crystal where the flatness of a base affects an orientation, like a ferroelectric liquid crystal. However, like the present invention, in the case to the extent that the two colored layers are stacked, this is a level that hardly influences the flatness of the substrate and also the liquid crystal layer.

[0029]

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In this way, the present invention is characterized in that the light shielding mask is formed by the stacked film (R + B) consisting of the two colored-layers. As a result, a step of forming a black matrix can be omitted, reducing the number of steps.

[0030]

However, the cross-sectional views shown in Fig. 1(B) ~ Fig.1(C) are examples which are not particularly limited, and for example, a structure shown in Fig. 2(B) ~Fig.2(C) may be taken. Fig. 2(B) is an example in which after a colored layer (G) 23 is formed over an opposing substrate 20, by stacking a colored layer (R) 22 and a colored layer (B) 21, a light shielding portion 25 (R + B), a pixel opening (B) 27, a pixel opening (R) 28, and a pixel opening (G) 29 are formed. Therefore, in Fig. 2(C), after the colored layer (R) 22 is formed over the opposing substrate 20, the colored layer (B) 21 is stacked, and the light shielding portion (B + R) 25 is formed. Further, the colored layers are covered by a leveling film 24.

[0031]

Besides, Fig. 4 shows a positional relationship of a wiring between the pixel

electrodes, the pixel electrodes, and the colored layers. Fig. 4(A) corresponds to Fig. 1. Fig. 4(A) is an example where a colored layer (R) 59 is formed such that a portion thereof overlaps with an end portion of a colored layer (B) 58 above a source wiring 50 in order to shield a gap between a pixel electrode 51 and a pixel electrode 52 from light. The overlapping portion of the colored layer (B) 58 and the colored layer (R) 59 may be provided above the source wiring 50. Note that, in Fig. 4(A), reference numerals 53 and 55 indicate orientation films, reference numeral 54 indicates a liquid crystal, reference numeral 56 indicates an opposing electrode, and reference numeral 57 indicates a leveling film.

10 [0032]

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The structure as shown in Fig. 4(B) may be implemented. Fig. 4(B) corresponds to Fig. 2. Fig. 4(B) is an example where a colored layer (B) 68 is formed such that a portion thereof overlaps with an end portion of a colored layer (R) 69 above a source wiring 60, in order to shield a gap between a pixel electrode 61 and a pixel electrode 62 from light.

[0033]

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Note that, without being limited to the examples shown in Figs. 4(A) (B), the overlapping portion formed by patterning of the two colored layers may be enlarged to provide the light shielding portion also in peripheral portions of the source wiring. Using this light shielding portion hides light leakage that occurs at the time of source line inversion driving, so that contrast is improved.

[0034]

Further, the light that has passed through the pixel openings $17 \sim 19$ is colored in the corresponding colors by the single layered colored layers $11 \sim 13$, and recognized

by the observer. Note that, Fig. 1(B) shows the sectional structure where the pixel opening in Fig. 1(A) is cut along the chain line (A1-A1'). As shown in Fig. 1(C), the single layered colored layers 11 ~ 12 are sequentially formed over the opposing substrate 10. Further, the leveling film 14 covering these colored layers 11 ~ 12 is formed.

[0035]

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In the pixel opening, as with conventional practice shown in Fig. 19, the blue colored layer shows a transmittivity exceeding 85% near 450 nm. Further, the green colored layer shows a transmittivity exceeding 80% near 530 nm. Further, the red colored layer shows a transmittivity exceeding 90% near 600 ~ 800 nm.

[0036]

Here, because an example of the transmission type liquid crystal display device is given, light incident to the pixel openings $17 \sim 19$ passes through the pixel electrode and the liquid crystal layer, and after passing through the respective single layered colored layers $11 \sim 13$, the lights of respective colors are extracted to be recognized by the observer.

[0037]

Further, for the colored layers $11 \sim 13$, a diagonal mosaic alignment, a triangle mosaic alignment, an RGBG four pixel alignment, an RGBW four pixel alignment, or the like as well as a most simple stripe pattern can be used.

[0038]

With regard to the invention of this specification with the above structures, further detailed description is done referring to the embodiments below.

[0039]

[Embodiment]

[Embodiment 1]

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One embodiment of the present invention will be described hereinbelow, taking a manufacturing of an opposing substrate which will be employed for an active matrix liquid crystal display device for an example. Fig. 1 is a schematic view showing an opposing substrate with a colored layer formed according to the present invention.

[0040]

First, as the opposing substrate 10 having a light transmission property, a glass substrate, such as barium borosilicate glass or aluminum borosilicate glass represented by #7059 glass or #1737 glass of Corning Incorporated or the like, is prepared. In addition to the above, a light transmission type substrate such as a quartz substrate and a plastic substrate can also be used.

[0041]

Next, an organic photosensitive material (CRY-8000: COLOR MOSAIC made by Fuji Film Olin Corp.) is applied on the opposing substrate 10, and by a photolithography method, this organic photosensitive material is patterned in a grid-shape as shown in Fig. 1(A) to form the green colored layer (G) 13. Note that this region becomes the pixel opening 19 with respect to the green colored layer (G) 13. [0042]

Next, an organic photosensitive material (CGY-8000: COLOR MOSAIC made by Fuji Film Olin Corp.) is applied to a predetermined position, and by a photolithography method, this organic photosensitive material is patterned as shown in Fig. 1(A) to form the blue colored layer (B) 11 in the predetermined position.

[0043]

Next, an organic photosensitive material (CM-8000: COLOR MOSAIC made by Fuji Film Olin Corp.) is applied to a predetermined position, and by a photolithography method, this organic photosensitive material is patterned as shown in Fig. 1(A) to form the red colored layer (R) 12. As shown in Fig. 1, a portion of the blue colored layer (B) 11 overlaps a portion of the red colored layer (R) 12 to form the light shielding portion 15. This light shielding portion 15 is designed to shield at least a pixel TFT, a gate wiring (not shown), and a source wiring (not shown). On the other hand, as shown in Fig. 1(B), in the blue colored layer (B) 11, a region which does not overlap with the red colored layer (R) 12 becomes the blue pixel opening (B) 17. Further, in the red colored layer (R) 12, the region which does not overlap with the blue colored layer (B) 11 becomes the red pixel opening (R) 18.

[0044]

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Note that, the light shielding portion 15 is formed to overlap with a TFT channel forming region when it is adhered together with an element substrate on which a TFT is provided.

[0045]

Thus, by three times of the photolithography method, the pixel openings $17 \sim 19$, and the light shielding portion 15 can be formed.

[0046]

Subsequently, the leveling film 14 covering the respective colored layers is

formed. Since between the region where the colored layer is a single layer and the region where the two colored layers are stacked, a step of about $1 \sim 1.5 \,\mu m$ arises, the

leveling film 14 needs to have a film thickness of 1 μm or more, preferably 2 $\mu m. \;\;$ As

for this leveling film 14, an organic material having a light transmission property, for

example, an organic resin material such as polyimide, acryl, polyamide, polyimide amide, or BCB (benzocyclobutene) can be used. However, if flatness is not problematic, this leveling film need not be provided.

[0047]

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Note that, although in this embodiment the organic photosensitive material is applied and patterned into the desired shape by the photolithography method to obtain the respective colored layers 11 ~ 13, it is needless to say that there is no particular limitation to the above manufacturing method.

[0048]

Hereafter, although not shown, an opposing electrode formed of a transparent conductive film is formed on the leveling film, and further thereon, an orientation film for orienting a liquid crystal is formed, and furthermore, if necessary, an orientation process is performed.

[0049]

Using the opposing substrate thus obtained, an active matrix liquid crystal display device is manufactured.

[0050]

[Embodiment 2]

In Embodiment 1, an example where the green colored layer (G) 13, the blue colored layer (B) 11, and the red colored layer (R) 12 are sequentially formed is shown, but an example where the colored layers are formed in an order different from that of Embodiment 1 is shown below.

[0051]

Fig. 2(A) is an example where first the colored layer (G) 23 is formed and the

colored layer (R) 22 and the colored layer (B) 21 are stacked. Note that, Fig. 2(B) corresponds to a cross sectional structural diagram cut along the chain line A3-A3' of Fig. 2(A), and Fig. 2(C) corresponds to a cross-sectional structural diagram cut along the chain line A4-A4' of Fig. 2(A).

5 [0052]

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As the opposing substrate 20, the substrate used in Embodiment 1 can be used.

[0053]

First, an organic photosensitive material (CRY-8000: COLOR MOSAIC made by Fuji Film Olin Corp.) is applied over the opposing substrate 20, and by a photolithography method, this organic photosensitive material is patterned in a grid-shape as shown in Fig. 2(A) to form the green colored layer (G) 23. Note that this region becomes the pixel opening 29 with respect to the green colored layer (G) 23. [0054]

Next an organic photosensitive material (CGY-8000: COLOR MOSAIC made by Fuji Film Olin Corp.) is applied to a predetermined position, and by a photolithography method, this organic photosensitive material is patterned as shown in Fig. 2(A) to form the red colored layer (R) 22 in a predetermined position.

Next an organic photosensitive material (CM-8000: COLOR MOSAIC made by Fuji Film Olin Corp.) is applied to the predetermined position, and by a photolithography method, this organic photosensitive material is patterned into a shape as shown in Fig. 2(A) to form the blue colored layer (B) 21. As shown in Fig. 2(B) and Fig. 2(A), a portion of this red colored layer (R) 22 overlaps a portion of the blue colored layer (B) 21 to form the light shielding portion 25. On the other hand, as

shown in Fig. 2(B), in the blue colored layer (B) 21, a region which does not overlap with the red colored layer (R) 22 becomes the blue pixel opening (B) 27. Further, in the red colored layer (R) 22, the region which does not overlap with the blue colored layer (R) 21 becomes the red pixel opening (R) 28.

[0056]

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Note that, the light shielding portion 25 is formed to overlap with a TFT channel forming region when it is adhered together with an active matrix substrate on which the TFT is provided.

[0057]

Thus, by three times of the photolithography method, the pixel openings $27 \sim 29$, and the light shielding portion 25 can be formed.

[0058]

Subsequently, the leveling film 24 covering the respective colored layers is formed. Since between the region where the colored layer is a single layer and the region where the two colored layers are stacked, a step of about $1\sim1.5~\mu m$ arises, the leveling film 24 needs to have a film thickness of $1~\mu m$ or more, preferably $2~\mu m$. As for the leveling film 24, an organic material having a light transmission property, for example, an organic resin material such as polyimide, acryl, polyamide, polyimide amide, or BCB (benzocyclobutene) can be used. However, if flatness is not problematic, this leveling film need not be provided.

[0059]

Note that, although in this embodiment the organic photosensitive material is applied and patterned into the desired shape by the photolithography method to obtain the respective colored layers $21 \sim 23$, it is needless to say that there is no particular

limitation to the above manufacturing method.

[0060]

Hereafter, although not shown, an opposing electrode formed of a transparent conductive film is formed on the leveling film, and further thereon, an orientation film for orienting a liquid crystal is formed, and furthermore, if necessary, an orientation process is performed.

[0061]

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Using the opposing substrate thus obtained, an active matrix liquid crystal display device is manufactured.

10 [Embodiment 3]

In this embodiment, a method of manufacturing an active matrix substrate is described using Fig. 5 ~ Fig.11.

[0062]

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In this embodiment, a description will be made of a manufacturing method of the active matrix substrate (also referred to as an element substrate) which is stuck with the opposing substrate obtained in Embodiment 1 or Embodiment 2. Here, a method of simultaneously forming, over the same substrate, a pixel portion and TFTs (n-channel TFT and p-channel TFT) of a driver circuit to be provided in a periphery of the pixel portion, is described in detail.

20 [0063]

First, in this embodiment, a substrate 400 which is made from glass such as barium borosilicate glass or aluminum borosilicate glass represented by #7059 glass or #1737 glass of Corning Incorporated is used. Note that, as the substrate 400, a quartz substrate may be used. Instead, a plastic substrate having heat resistance to the process

temperature of this embodiment may also be used. There is no particular limitation, as long as a substrate with a transparent property is used.

[0064]

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Then, a base film 401 formed of an insulating film, such as a silicon oxide film, a silicon nitride film or a silicon nitride oxide film, is formed over the substrate 400. In this embodiment, although a two-layer structure is used as the base film 401, a single-layer film or a stacked structure of two or more layers of the insulating film may be used. As a first layer of the base film 401, a silicon oxynitride film 401a is formed into a thickness of $10 \sim 200$ nm (preferably $50 \sim 100$ nm) by a plasma CVD method with SiH₄, NH₃, and N₂O as reaction gases. In this embodiment, the silicon oxynitride film 401a (composition ratio Si = 32%, O = 27%, N = 24%, H = 17%) having a film thickness of 50 nm is formed. Then, as a second layer of the base film 401, a silicon oxynitride film 401b is formed so as to be stacked thereon into a thickness of $50 \sim 200$ nm (preferably $100 \sim 150$ nm) by a plasma CVD method with SiH₄ and N₂O as reaction gases. In this embodiment, the silicon oxynitride film 401b (composition ratio Si = 32%, O = 59%, N = 7%, H = 2%) having a film thickness of 100 nm is formed.

Subsequently, semiconductor layers 402 ~ 406 are formed on the base film. As for the semiconductor layers 402 ~ 406, after a semiconductor film having an amorphous structure is formed by a known method (a sputtering method, an LPCVD method, a plasma CVD method, or the like), a crystalline semiconductor film which is obtained by a known crystallization process (a laser crystallization method, a thermal crystallization method using a catalyst such as nickel, or the like) is patterned into a desired shape to obtain the semiconductor layers. The

semiconductor layers 402 ~ 406 are formed into a thickness of 25 ~ 80 nm (preferably 30 ~ 60 nm). The material of the crystalline semiconductor film is not limited, but it is preferable to form the film using silicon, a silicon germanium (SiGe) alloy, or the like. In this embodiment, after a 55 nm-thick amorphous silicon film is formed by a plasma CVD method, a nickel-containing solution is held on the amorphous silicon film. After a dehydrogenation process (500 °C, for one hour) is performed to the amorphous silicon film, a thermal crystallization (550 °C, for four hours) is performed, and a laser anneal treatment for further improving crystallization is performed to form a crystalline silicon film. Then, by a patterning process on this crystalline silicon film using a photolithography method, the semiconductor layers 402 ~ 406 are formed.

[0066]

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Further, after the formation of the semiconductor layers 402 ~ 406, doping with a minute amount of impurity element (boron or phosphorus) may be performed to control the threshold of the TFT.

[0067]

Besides, in the case where the crystalline semiconductor film is manufactured by the laser crystallization method, a pulse oscillation type or continuous-wave type excimer laser, YAG laser, or YVO₄ laser can be used. In the case where those lasers are used, it is appropriate to use a method in which laser light radiated from a laser oscillator is condensed by an optical system into a linear shape and is emitted to the amorphous semiconductor film. Although a condition of the crystallization is properly selected by an operator, in the case where the excimer laser is used, a pulse repetition rate is set to 30 Hz, and a laser energy density is set to 100 ~ 400 mJ/cm² (typically 200 ~ 300 mJ/cm²). Instead, in the case where the YAG laser is used, it is appropriate that

the second harmonic is used, a pulse repetition rate is set to $1 \sim 10$ kHz, and laser energy density is set to $300 \sim 600$ mJ/cm² (typically, $350 \sim 500$ mJ/cm²). Then, laser light condensed into a linear shape with a width of $100 \sim 1000$ μ m, for example, 400 μ m is emitted to the whole surface of the substrate, and an overlapping ratio (overlap ratio) of the linear laser light at this time may be set to $80 \sim 98\%$.

[0068]

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A gate insulating film 407 covering the semiconductor layers $402 \sim 406$ is then formed. The gate insulating film 407 is formed of an insulating film containing silicon by a plasma CVD method or a sputtering method into a film thickness of from $40 \sim 150$ nm. In this embodiment, the gate insulating film 407 is formed of a silicon oxynitride film (composition ratio Si = 32%, O = 59%, N = 7%, H = 2%) into a thickness of 110 nm by a plasma CVD method. Of course, the gate insulating film is not limited to the silicon oxynitride film, and another insulating film containing silicon may be used as a single layer or a stacked structure.

[0069]

Besides, in the case where a silicon oxide film is used, the silicon oxide film can be formed by a plasma CVD method, TEOS (Tetraethyl Orthosilicate) and O_2 are mixed and discharged at a high frequency (13.56 MHz) power density of $0.5 \sim 0.8$ W/cm² with a reaction pressure of 40 Pa and a substrate temperature of $300 \sim 400$ °C. The silicon oxide film thus manufactured can be given good characteristics as the gate insulating film by subsequent thermal annealing at $400 \sim 500$ °C.

[0070]

Then, as shown in Fig.5(A), over the gate insulating film 407, a first conductive film 408 with a film thickness of $20 \sim 100$ nm and a second conductive film 409 with a

film thickness of 100 ~ 400 nm are formed to be stacked. In this embodiment, the first conductive film 408 formed of a TaN film with a film thickness of 30 nm and the second conductive film 409 formed of a W film with a film thickness of 370 nm are formed to be stacked. The TaN film is formed by a sputtering method in which sputtering is performed with a Ta target under a nitrogen containing atmosphere. Besides, the W film is formed by the sputtering method with a W target. In addition, the formation by a thermal CVD method using tungsten hexafluoride (WF₆) is also In any case, it is necessary to make resistance lower for use as the gate electrode, and it is preferred that resistivity of the W film is set to less than or equal to 20 μΩcm. Enlargement of crystal grains enables the resistivity of the W film to decrease; however, in the case where many impurity elements such as oxygen are contained within the W film, the crystallization is inhibited and the resistance becomes higher. Therefore, in this embodiment, by forming the W film by a sputtering method using the W target having a high purity (purity of 99.9999%), and in addition, in sufficient consideration for prevention of incorporation of impurities within gas phase during the film formation, a resistivity of $9 \sim 20 \,\mu\Omega$ cm could be realized.

[0071]

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Note that, in this embodiment, although the first conductive film 408 is formed of TaN and the second conductive film 409 is formed of W, the material is not particularly limited and either film may be formed of an element selected from Ta, W, Ti, Mo, Al, Cu, Cr, and Nd, or an alloy material or a compound material containing the above element as its main ingredient. Alternatively, a semiconductor film typified by a polycrystalline silicon film doped with an impurity element such as phosphorus may be used. Further, an AgPdCu alloy may be used. Instead, a combination in which the

first conductive film is formed of a tantalum (Ta) film and the second conductive film is formed of a W film, a combination in which the first conductive film is formed of a titanium nitride (TiN) film and the second conductive film is formed of the W film, a combination in which the first conductive film is formed of a tantalum nitride (TaN) film and the second conductive film is formed of an Al film, or a combination in which the first conductive film is formed of the tantalum nitride (TaN) film and the second conductive film is formed of a Cu film may be employed.

[0072]

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Next, masks 410 ~ 415 formed of resist are formed using a photolithography method, and a first etching process for forming electrodes and wirings is conducted. The first etching process is conducted under the first and second etching conditions. In this embodiment, as the first etching condition etching is conducted using an ICP (Inductively Coupled Plasma: inductively coupled plasma) etching method, in which CF₄, Cl₂ and O₂ are used as etching gases, the gas flow rate of the respective gases is set to 25/25/10 (sccm), and an RF (13.45 MHz) power of 500W is applied to a coil-shaped electrode with a pressure of 1 Pa to generate plasma. Here, a dry etching device using ICP (Model E645-□ICP) of Matsushita Electric Industrial Co., Ltd. is used. The RF (13.56 MHz) power of 150 W is also applied to the substrate side (sample stage) and a substantially negative self bias voltage is applied. Based on this first etching condition, the W film is etched to make an end portion of the first conductive layer into a tapered shape.

[0073]

Thereafter, without removing the masks $410 \sim 415$ formed of the resist, the etching condition is changed into a second etching condition, in which CF₄ and Cl₂ are

used as the etching gases, the gas flow rate of the respective gases is set to 30/30 (sccm), and an RF (13.56 MHz) power of 500 W is applied to the coil type electrode under a pressure of 1 Pa, to generate plasma, and etching is performed for about 30 seconds. An RF (13.56 MHz) power of 20 W is also applied to the substrate side (sample stage) and a substantially negative self bias voltage is applied. In the second etching condition, in which CF_4 and Cl_2 are mixed, the W film and the TaN film are etched in the same degree. Note that, in order to perform the etching without leaving a residue on the gate insulating film, it is appropriate that an etching time be increased at a rate of about $10 \sim 20\%$.

10 [0074]

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In the above first etching process, by making the masks formed of the resist have a suitable shape, end portions of the first conductive layer and the second conductive layer become the tapered shape due to the effect of the bias voltage applied to the substrate side. The angle of this tapered portion becomes $15 \sim 45^{\circ}$. In this way, first shape conductive layers $417 \sim 422$ consisting of the first conductive layers and the second conductive layers (first conductive layers $417a \sim 422a$ and second conductive layers $417b \sim 422b$) are formed by the first etching process. Reference numeral 416 is a gate insulating film, and regions which are not covered with the first shape conductive layers $417 \sim 422$ are etched by about $20 \sim 50$ nm so that thinned regions are formed.

20 [0075]

Then, a first doping process is performed without removing the masks formed of the resist, and an impurity element imparting an n-type is added to the semiconductor layers (Fig. 5(B)). The doping process may be performed by an ion doping method or an ion implanting method. The ion doping method is performed under a condition in

which a dose amount is $1 \times 10^{13} \sim 5 \times 10^{15}$ atoms/cm², and an acceleration voltage is 60 ~100 keV. In this embodiment, the dose amount is set to 1.5×10^{15} atoms/cm² and the acceleration voltage is set to 80 keV. As the impurity element imparting the n-type, an element belonging to group 15, typically phosphorus (P) or arsenic (As) is used, but phosphorus (P) is used here. In this case, the conductive layers 417 ~ 421 become the masks against the impurity element imparting the n-type, and high concentration impurity regions 423 ~ 427 are formed in a self aligning manner. The impurity element imparting the n-type in a concentration range of $1 \times 10^{20} \sim 1 \times 10^{21}$ atoms/cm³ is added to the high concentration impurity regions 423 ~ 427.

[0076]

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[0077]

Next, a second etching process is performed without removing the masks formed of the resist. Here, CF_4 , CI_2 and O_2 are used as the etching gases, and the W film is selectively etched. At this time, by the second etching process, first conductive layers $428b \sim 433b$ are formed. On the other hand, the second conductive layers $417a \sim 422a$ are hardly etched, and second conductive layers $428a \sim 433a$ are formed. Next, a second doping process is conducted to obtain a state as shown in Fig. 5(C). The doping is performed such that the second conductive layers $417a \sim 422a$ are used as the masks against the impurity element, and the impurity element is added to the semiconductor layers under the tapered portions of the first conductive layers. In this way, impurity regions $434 \sim 438$ overlapping with the first conductive layers are formed. The concentration of phosphorus (P) added to the impurity regions has a gentle concentration gradient according to the film thickness of the tapered portions of the first conductive layers. Note that, in the semiconductor layer overlapping with the tapered

portion of the first conductive layer, an impurity concentration is somewhat lowered from the end portion of the tapered portion of the first conductive layer toward the inside, but is at the same level of the concentration. Further, the impurity element is added to the first impurity regions $423 \sim 427$ to form impurity regions $439 \sim 443$.

[0078]

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Next, a third etching process is performed without removing the masks formed of the resist as shown in Fig. 6(A). In the third etching process, the tapered portion of the first conductive layer is partially etched, to reduce the region overlapping with the semiconductor layer. The third etching is performed using CHF₃ as the etching gas with a reactive ion etching method (RIE method). With the third etching, first conductive layers $444 \sim 449$ are formed. At this time, the insulating film 416 is simultaneously etched to form insulating films $450a \sim 450d$ and 451.

By the third etching, impurity regions (LDD regions) $434a \sim 438a$ that do not overlap with the first conductive layers $444 \sim 448$ are formed. Note that, impurity regions (GOLD regions) $434b \sim 438b$ still are overlapped with the first conductive layers $444 \sim 448$.

[0080]

[0079]

In this way, in this embodiment, a difference between the impurity concentration in the impurity regions (GOLD regions) 434b ~ 438b which overlap with the first conductive layers 444 ~ 448 and the impurity concentration in the impurity regions (LDD regions) 434a ~ 438a which do not overlap with the first conductive layers 444 ~ 448 can be made small, thereby improving reliability.

[0081]

Then, as shown in Fig. 6(B), after removing the masks formed of the resist, new masks 452 ~ 454 formed of the resist are formed, and a third doping process is performed. With this third doping process, impurity regions 455 ~ 460, in which an impurity element imparting a conductivity type opposite to the above one conductivity type is added, are formed in the semiconductor layer that becomes an active layer of a p-channel TFT. The second conductive layers 428a ~432a are used as the masks with respect to the impurity element, and an impurity element imparting a p-type is added to form the impurity regions in a self aligning manner. In this embodiment, the impurity regions $455 \sim 460$ are formed by an ion doping method using diborane (B_2H_6). At the time of performing the third doping process, the semiconductor layers forming the n-channel TFTs are covered with the masks 452 ~ 454 formed of the resist. Although the impurity regions 455 ~ 460 are doped with phosphorus with different concentrations respectively through the first doping process and the second doping process, the doping process is performed so that the concentration of the impurity element imparting the p-type in any of the regions falls within the range of 2×10^{20} $\sim 2 \times 10^{21}$ atoms/cm³; accordingly, the regions function as source regions and drain regions of the p-channel TFTs, and therefore no problem is caused. In this embodiment, since a portion of the semiconductor layer to be the active layer of the p-channel TFT is exposed, there is an advantage that the impurity element (boron) is easily added.

20 [0082]

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By the steps up to here, the impurity regions are formed in the respective semiconductor layers.

[0083]

Subsequently, the masks 452 ~ 454 formed of the resist are removed, and a first

interlayer insulating film 461 is formed. This first interlayer insulating film 461 is formed of an insulating film containing silicon by a plasma CVD method or a sputtering method into a thickness of 100 ~ 200 nm. In this embodiment, a silicon oxynitride film with a film thickness of 150 nm is formed by the plasma CVD method. Of course, the first interlayer insulating film 461 is not particularly limited to the silicon oxynitride film, but another insulating film containing silicon may be used as a single layer or a stacked structure.

[0084]

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Then, as shown in Fig. 6(C), an activation process of the impurity elements added to the respective semiconductor layers is performed. This activation step is carried out by a thermal annealing method using a furnace annealing oven. The thermal annealing method may be performed in a nitrogen atmosphere having an oxygen concentration of 1 ppm or less, preferably 0.1 ppm or less and at $400 \sim 700$ °C, typically $500 \sim 550$ °C; in this embodiment, the activation process is carried out with heat treatment at 550 °C for 4 hours. Note that, other than the thermal annealing method, a laser annealing method, or a rapid thermal annealing method (RTA method) can be applied.

[0085]

Note that, in this embodiment, at the same time as the above activation process, nickel used as the catalyst for crystallization is gettered to the impurity regions 439, 441, 442, 455 and 458 containing phosphorus at high concentration; therefore the nickel concentration of the semiconductor layers which mainly become the channel forming regions is lowered. The TFT having the channel forming region thus formed is decreased in an off current, and high electric field mobility can be obtained because of

good crystallinity, thereby attaining satisfactory characteristics.

[0086]

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Further, the activation process may be performed before forming the first interlayer insulating film. However, in the case where a wiring material used is weak against heat, the activation process is preferably performed after the interlayer insulating film (an insulating film containing silicon as its main ingredient, for example, silicon nitride film) is formed to protect the wiring or the like as in this embodiment.

Besides, a top view of the pixel portion after the activation process described above is shown in Fig. 7. Note that, the same reference numerals are used to indicate the parts corresponding to Fig. 5 and Fig. 6. A dash line C-C' in Fig. 6 corresponds to a sectional view taken along the line C-C' in Fig. 7. Also, a dash line D-D' in Fig. 6 corresponds to a sectional view taken along the dash line D-D' in Fig. 7.

[0088]

In addition, heat treatment at 300 ~ 550 °C for 1 ~ 12 hours is performed in an atmosphere containing hydrogen of 3 ~ 100%, to perform a step of hydrogenating the semiconductor layers. In this embodiment, the heat treatment is performed at 410 °C for 1 hour in a nitrogen atmosphere containing hydrogen of about 3%. This step is a step of terminating dangling bonds in the semiconductor layer by the hydrogen contained in the interlayer insulating film. As another means for hydrogenation, plasma hydrogenation (using hydrogen excited by plasma) may be carried out.

Instead, in the case of using the laser annealing method as the activation process, the laser light, such as the excimer laser or the YAG laser, is preferably emitted after the aforementioned hydrogenation.

[0090]

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A second interlayer insulating film 462 formed of an organic resin and wirings 463 ~ 471 connected to the respective semiconductor layers are formed; then, the patterning process is performed using a photo mask to form a transparent conductive film 472 over the entire surface, and a state shown in Fig. 8 can be obtained.

[0091]

As the material for the transparent conductive film, indium oxide (In₂O₃), an alloy of indium oxide and tin oxide (In₂O₃-SnO₂; ITO film), or the like can be used by a sputtering method, a vacuum evaporation method, or the like. The etching process of such a material is performed with a hydrochloric acid based solution. Since the residue tends to be generated in etching of especially the ITO film, the alloy of indium oxide and zinc oxide (In₂O₃-ZnO) may be used to improve etching processability. The alloy of indium oxide and zinc oxide is excellent in surface smoothness, and is also excellent in heat stability to the ITO film; therefore, even when Al is used for a drain wiring and a capacitance connection wiring, a corrosion reaction with Al which is contacted at the surface can be prevented. Similarly, zinc oxide (ZnO) is also an appropriate material, and further, zinc oxide added with gallium (Ga) (ZnO: Ga) or the like can be used in order to increase the transmittivity of visible light and conductivity.

20 [0092]

In the manner as described above, a driving circuit 306 including an n-channel TFT 301, a p-channel TFT 302, and an n-channel TFT 303, and a pixel portion 307 including a pixel TFT 304 and a storage capacitor 305 can be formed on the same substrate. In the present specification, such a substrate is called the active matrix

substrate for convenience.

[0093]

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The n-channel TFT 301 of the driving circuit 306 includes a channel forming region 472, the impurity region 434b (GOLD region) overlapping with the second shape conductive layer 428 forming the gate electrode, the impurity region 434a (LDD region) formed outside the gate electrode, and the impurity region 439 functioning as a source region or a drain region. The p-channel TFT 302 includes a channel forming region 473, an impurity region 457 overlapping with the second shape conductive layer 429 forming the gate electrode, an impurity region 456 formed outside the gate electrode, and the impurity region 455 functioning as a source region or a drain region. The n-channel TFT 303 includes a channel forming region 474, the impurity region 436b (GOLD region) overlapping with the second shape conductive layer 430 forming the gate electrode, an impurity region 436a (LDD region) formed outside the gate electrode, and the impurity region 441 functioning as a source region or a drain region.

15 [0094]

The pixel TFT 304 of the pixel portion includes a channel forming region 475, the impurity region 437b (GOLD region) overlapping with the second shape conductive layer 431 forming the gate electrode, an impurity region 437a (LDD region) formed outside the gate electrode, and the impurity region 442 functioning as the source region or the drain region. Besides, the impurity elements imparting the p-type are added to the respective semiconductor layers 458 ~ 460 functioning as one of the electrodes of the storage capacitor 305 at the same concentration as the impurity regions. The storage capacitor 305 is formed of the electrodes 432b and 448 and the semiconductor layers 458 ~ 460 using the insulating film (the same film as the gate insulating film) as a

dielectric member.

[0095]

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A top view of the pixel portion of the active matrix substrate manufactured in this embodiment is shown in Fig. 9. Note that, the same reference numerals are used to indicate the parts corresponding to Fig. 5 ~ Fig. 8. A dash line A-A' in Fig. 9 corresponds to a sectional view taken along the line A - A' in Fig. 8. Also, a dash line B-B' in Fig. 9 corresponds to a sectional view taken along the dash line B-B' in Fig. 8.

Like this, the active matrix substrate having a pixel structure according to this embodiment is characterized in that electrodes 431b and 447 a part of which functions as the gate electrode and a gate wiring 470 are formed on different layers, and that light shielding of the semiconductor layers is performed by the gate wiring 470.

[0097]

Further, in the pixel structure of this embodiment, the end portion of the pixel electrode is arranged and formed so as to overlap with the source wiring so that the gap between the pixel electrodes is shielded from light without using a black matrix.

[0098]

In addition, in accordance with the process shown in this embodiment, the number of photo masks needed for the manufacture of the active matrix substrate can be six (a semiconductor layer patterning mask, a first wiring patterning mask (including the electrodes 431b and 447, the electrodes 432b and 448, and the source wiring 433b and 449), a patterning mask of the source region and drain region formation of the p-type TFT, the patterning mask of a contact hole formation, a second wiring patterning mask (including the connection electrode 467, the connection electrode 469, and the gate

wiring 470), and a pixel electrode patterning mask. As a result, contribution to shortening of the process, to reduction in manufacturing costs, and to improvement in yield is possible.

[0099]

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Further, the liquid crystal display device can be obtained using the active matrix substrate fabricated in this embodiment in accordance with the steps in Embodiment 1, Embodiment 2, Embodiment 4 and Embodiment 5.

[0100]

[Embodiment 4]

In this embodiment, a process of manufacturing an active matrix liquid crystal display device from the active matrix substrate manufactured in Embodiment 3 will be described hereinbelow. Fig. 10 is used for an explanation.

[0101]

First, in accordance with Embodiment 3, after the active matrix substrate in the state shown in Fig. 8 is obtained, an orientation film 567 is formed on the active matrix substrate as shown in Fig. 8, and a rubbing process is performed. Note that, in this embodiment, before the formation of the orientation film 567, a columnar spacer 572 for maintaining a gap between the substrates is formed at a desired position by patterning of an organic resin film such as an acrylic resin film. Further, spherical spacers may be scattered on the entire surface of the substrate in place of the columnar spacer.

[0102]

Next, an opposing substrate 569 is prepared. A first colored layer 570, a second colored layer 571, and a leveling film 573 are formed on the opposing substrate

569. In accordance with Embodiment 1, a colored layer (B) is used as the first colored layer 570, and the colored layer (R) is used as the second colored layer 571. The first colored layer 570 and the second colored layer 571 are partially overlapped with each other, thereby forming a light shielding portion.

[0103]

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Subsequently, an opposing electrode 576 is formed in a pixel portion, and an orientation film 574 is formed on the entire surface of the opposing substrate. Then, the orientation process is performed.

[0104]

Then, the active matrix substrate on which the pixel portion and a driver circuit are formed is stuck with the opposing substrate by a sealing material 568. In the sealing material 568, a filler is mixed, and the two substrates are stuck together, keeping a uniform gap by the effect of this filler and the columnar spacer 572. Thereafter, a liquid crystal material is injected between both the substrates, and completely sealed by a sealant (not shown). A known liquid crystal material may be used as the liquid crystal material. Thus the active matrix liquid crystal display device shown in Fig. 10 is completed.

[0105]

In this embodiment, the substrate shown in Embodiment 3 is used. Accordingly, in Fig. 9 showing a top view of the pixel portion in accordance with Embodiment 3, light shielding must be performed at least in the gap between the gate wiring 470 and the pixel electrode 472, a gap between the gate wiring 470 and the connection electrode 469, a gap between the connection electrode 469 and the gate wiring 470, a gap between the gate wiring 470 and the connection electrode 479, gaps

between the gate wiring 470 and the source wirings 433b, 449, gaps between the source wirings 433b, 449 and the semiconductor layer 474 and a gap between the source wiring 473 and the semiconductor layer 474. In this embodiment, the opposing substrate is stuck, so that the light shielding portion overlaps with the positions which need to be shielded from light.

[0106]

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Note that, Fig. 11 is a schematic view showing a part of the pixel portion of the completed liquid crystal display device. In Fig. 11, the colored layer (R) 12 is formed so as to overlap with the pixel electrode 472 indicated by chain lines. Note that, in Fig. 11, the same reference numerals are used for the parts corresponding to those in Fig. 1(A). Besides, the gap between the pixel electrode 472 and its adjacent pixel electrode 475 is shielded from light by the light shielding portion 15. This light shielding portion 15 is formed of the colored layer (B) 11 and the colored layer (R) 12 which are overlapped with each other. Further, this light shielding portion 15 also shields the pixel TFT of the adjacent pixel (G) from light. Simultaneously, pattering is performed so that the colored layer (B) 11 and the colored layer (R) 12, with which the source wirings 433b and 449 overlap, overlap with each other.

[0107]

In this way, without forming a black mask, shielding the gaps between the respective pixels from light by the light shielding portion 15 enables reduction in the number of steps.

[0108]

In this embodiment, the colored layer (B) as the first colored layer 570 and the colored layer (R) as the second colored layer 571 are used, but the colored layer (R) as

the first colored layer 570 and the colored layer (B) as the second colored layer 571 may be used.

[Embodiment 5]

With a top view of Fig. 12, a structure of the active matrix liquid crystal display device (Fig. 10) obtained by Embodiment 4 is described. Note that, the same reference numerals are used for the parts corresponding to those in Fig. 10.

[0109]

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In Fig. 12 showing the top view, an active matrix substrate 201, on which a pixel portion, a driver circuit, an external input terminal 203 for adhering an FPC (flexible printed circuit: Flexible Printed Circuit), a wiring 204 for connecting the external input terminal to the input portion of each circuit, and the like are formed, is stuck with an opposing substrate 202, on which the colored layer and the like are formed, by the sealing material 568.

[0110]

On top surfaces of a gate wiring driver circuit 205 and a source wiring driver circuit 206, a red color filter or a light shielding portion 207 where red and blue colored layers are stacked is formed on the opposing substrate side. Further, in a colored layer 208 formed on the opposing substrate side over the pixel portion 307, respective colored layers of red (R), green (G) and blue (B) are provided corresponding to respective pixels. When actually performing display, color display is performed with the three colors of the colored layers of red (R), green (G) and blue (B), but an arrangement of these colored layers of respective colors is arbitrary.

[0111]

Fig. 13(A) shows a cross-sectional view of the external input terminal 203

shown in Fig. 12 along the line E-E' The external input terminal is formed on the active matrix substrate side and is connected to a wiring 211 formed in the same layer as the gate wiring through an interlayer insulating film 210 by a wiring 209 to lower the interlayer capacitance and the wiring resistance and to prevent failure from disconnection. A transparent conductive film 217 formed by patterning of the transparent conductive film in Embodiment 4 is provided on the wiring 209.

[0112]

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Further, the external input terminal is stuck with an FPC formed of a base film 212 and a wiring 213 by an anisotropic conductive resin 214. Further, mechanical strength is increased by a reinforcement plate 215.

[0113]

Fig. 13(B) shows the detailed view and shows the cross-sectional view of the external input terminal shown in Fig. 13(A). The external input terminal provided on the active matrix substrate side is formed of the wiring 211 formed of the same layer as a first electrode and the source wiring and the wiring 209 formed of the same layer as a pixel electrode. Of course, this is only one example showing the structure of a terminal portion, and the external input terminal may be formed by just either one of the wirings. For example, in the case that the external input terminal is formed of the wiring 211 which is formed with the same layer as the first electrode and the source wiring, it is necessary to remove the interlayer insulating film formed thereon. The wiring 209 is formed of a three-layer structure of a Ti film 209a, an alloy film (an alloy film of Al and Ti) 209b, and a Ti film 209c. Further, the transparent conductive film 217 is formed on the Ti film 209a to improve the electric conductivity. The FPC is formed of the base film 212 and the wiring 213, and the wiring 213 and the transparent

conductive film 217 are stuck together with an anisotropic conductive adhesive comprised of the heat hardening type adhesive 214 and conductive particles 216 scattered therein, to form an electrical connecting structure.

[0114]

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The active matrix liquid crystal display device thus manufactured may be used as a display portion of various kinds of electronic equipment.

[0115]

[Embodiment 6]

Another example of the structures of an active matrix liquid crystal display device is described using a cross-sectional view of Fig. 14.

[0116]

An active matrix substrate 800 is featured in that a gate insulating film 801 and a source wiring 802 are simultaneously formed of tungsten, and that a gate wiring 803 and a connection wiring 804 are manufactured simultaneously of aluminum. The driver circuit 306 having the n-channel TFT 301, the p-channel TFT 302, and the n-channel TFT 303, the pixel portion 307 having the pixel TFT 304 and the storage capacitor 305 can be formed on the same substrate.

[0117]

The p-channel TFT 301 of the driver circuit 301 is formed with a single drain structure having a channel forming region 805, a source region 806 and a drain region 807 comprising p-type impurity regions with high concentration. The first n-channel TFT 302 comprises a channel forming region 808, an LDD region 809, a drain region 811 and a source region 812 in the island-shape semiconductor layer. The second n-channel TFT 303 of the driver circuit comprises a channel forming region 813 and an

LDD region 815 which partially overlaps with a gate electrode 814, in the island-shape semiconductor layer. The pixel TFT 304 has a channel forming region 816, an LDD region 817, and a source or drain region 818 in the island shaped semiconductor layer, and this source or drain region 818 forms an electrical connection with a pixel electrode 820. Further, the storage capacitor 305 forms an electrical connection with the pixel electrode 820 and the impurity region 819.

[0118]

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Throughout this specification, such a substrate is referred to as an active matrix substrate 800 for the sake of convenience.

10 [0119]

Next, an orientation film 867 is formed on the active matrix substrate 800, and an orientation process is performed. Note that, in this embodiment, before forming the orientation film 867, a columnar spacer 872 is formed in a desired position to maintain a gap between the substrates by patterning of an organic resin film such as an acrylic resin film. Alternatively, in place of the columnar spacer, a spherical spacer may be scattered on the entire surface of the substrate.

[0120]

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Next, an opposing substrate 869 is prepared. A first colored layer 870, a second colored layer 871, and a leveling film 873 are formed over the opposing substrate 869. In accordance with Embodiment 1, the colored layer (B) is used as the first colored layer 870, and the colored layer (R) is used as the second colored layer 871. The first colored layer 870 and the second colored layer 871 are partially overlapped with each other, thereby forming a light shielding portion. In the region other than the upper portion of the pixel electrode, the first colored layer 870 and the second colored

layer 871 are partially overlapped with each other to form the light shielding portion.

[0121]

Next, an opposing electrode 876 is formed in the pixel portion, an orientation film 874 is formed on the entire surface of the opposing substrate, and the orientation process is conducted.

[0122]

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Then, the active matrix substrate where the pixel portion and the driver circuit are formed, and the opposing substrate are stuck together with a sealing material 858. Thereafter, a liquid crystal 875 is injected between both of the substrates, and completely sealed by a sealant (not shown). A known liquid crystal material may be used as a liquid crystal material.

[0123]

Thus, the active matrix liquid crystal display device shown in Fig. 14 is completed.

[Embodiment 7]

In this embodiment, a liquid crystal display device having a reverse stagger type TFT is described using Fig. 15.

[0124]

A gate electrode 901 of a pixel TFT is formed on the substrate surface, and a semiconductor layer is formed with a first insulating layer 902 interposed therebetween. A source wiring 903 is formed on the same substrate surface as the gate electrode 901. A gate wiring 904 and a connection electrode 907 are formed on a second insulating layer 908 formed on the semiconductor layer. Then, the gate wiring 904 and a connection electrode 906 are respectively connected to the gate electrode 901 and the

semiconductor layer through contact holes. Further, the source wiring 903 and the semiconductor layer are connected by the connection wiring 907 formed in the same layer as the gate wiring 904. Besides, a protective film 905 and the leveling film 908 are formed.

5 [0125]

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A driver circuit 305 having a p-channel TFT 301 and an n-channel TFT 302 and a pixel portion 306 having a pixel TFT 303 and a storage capacitor 304 are formed over the same substrate. In the p-channel TFT 301 of the driver circuit 305, a channel forming region 909, and a source or drain region 910 are formed. In the n-channel TFT 302, a channel forming region 911, an LDD region 912, and a source or drain region 913 are formed. The pixel TFT 303 of the pixel portion 306 has a multi gate structure, and a channel forming region 914, a source or drain region 915, and an LDD region 916 are formed. The storage capacitor 304 is formed of a capacitor wiring 917, a semiconductor layer 918 and an insulating layer formed therebetween.

15 [0126]

A source or drain region 919 forms an electrical connection with a pixel electrode 920. Further, the pixel electrode 920 is connected with the semiconductor layer 917 of the storage capacitor 304.

[0127]

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Throughout this specification, such a substrate is referred to as an active matrix substrate 900 for the sake of convenience.

[0128]

Next, an orientation film 967 is formed on the active matrix substrate 900, and a rubbing process is performed. Note that, in this embodiment, before forming the

orientation film 967, a columnar spacer 972 is formed in the desired position to maintain a gap between the substrates by patterning of an organic resin film such as an acrylic resin film. Alternatively, in place of the columnar spacer, a spherical spacer may be scattered on the entire surface of the substrate.

5 [0129]

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Next, an opposing substrate 969 is prepared. A first colored layer 970, a second colored layer 971, and a leveling film 973 are formed over the opposing substrate 969. In accordance with Embodiment 1, the colored layer (B) is used as the first colored layer 970, and the colored layer (R) is used as the second colored layer 971. The first colored layer 970 is formed above the pixel electrode. In the region other than the upper portion of the pixel electrode, the first colored layer 970 and the second colored layer 971 are partially overlapped with each other to form a light shielding portion.

[0130]

Next, an opposing electrode 976 is formed in the pixel portion, an orientation film 974 is formed on the entire surface of the opposing substrate, and an orientation process is conducted.

[0131]

Then, the active matrix substrate where the pixel portion and the driver circuit are formed, and the opposing substrate are stuck together by a sealing material 958. Thereafter, a liquid crystal is injected between both of the substrates, and completely sealed by a sealant (not shown). A known liquid crystal material may be used as a liquid crystal material.

[0132]

One of advantages of forming the TFT as the reverse stagger type is that an LDD region which overlaps with the gate electrode in the n-channel TFT can be formed in a self-aligning manner by a process of exposing a back surface to light. Therefore, with the feature that the gate insulating film and the semiconductor layer can be continuously formed, characteristic variations in the TFT can be small.

[Embodiment 8]

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In this embodiment, referring to Fig. 16, a manufacturing method of a liquid crystal display device adopting a bottom gate TFT structure of a channel etch type is described. This TFT is featured in that patterning of a source region and a drain region and patterning of a pixel electrode are performed with the same photo mask.

[0133]

A structure of an active matrix substrate 1000 used in this embodiment is an active matrix substrate characterized by including a gate wiring 1002 formed on the insulating surface, an insulating film 1004b formed on the gate wiring, an amorphous semiconductor film 1014 formed on the insulating film, a source region 1015 and a drain region 1016 formed on the amorphous semiconductor film, a source wiring 1017 or an electrode 1018 formed on the source region or the drain region, and a pixel electrode 1019 formed on the electrode and characterized in that one end surface of the drain region 1016 or the source region 1015 substantially matches an end surface of the amorphous semiconductor film 1014 and an end surface of the electrode 1018.

[0134]

Next, an orientation film 1067 is formed on the active matrix substrate 1000, and an orientation process is performed. Note that, in this embodiment, although not shown, a columnar spacer or a spherical spacer may be used.

[0135]

Next, an opposing substrate 1069 is prepared. A first colored layer 1070, a second colored layer 1071, and a leveling film 1073 are formed over the opposing substrate 1069. In accordance with Embodiment 1, the colored layer (B) is used as the first colored layer 1070, and the colored layer (R) is used as the second colored layer 1071. The first colored layer 1070 and the second colored layer 1071 are partially overlapped with each other to form a light shielding portion.

[0136]

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Subsequently, an opposing electrode 1076 is formed in the pixel portion, an orientation film 1074 is formed on the entire surface of the opposing substrate, and the orientation process is performed.

[0137]

Then, the active matrix substrate on which the pixel portion and the driving circuit are formed is stuck with the opposing substrate by a sealing material (not shown). Thereafter, a liquid crystal 1068 is injected between both of the substrates and completely sealed by a sealant (not shown). A known liquid crystal material may be used as a liquid crystal material.

[0138]

Next a flexible printed circuit (Flexible Printed Circuit: FPC) is connected to an input terminal 1001 of a terminal portion. The FPC where a copper wiring 1028 is formed on an organic resin film 1029 such as polyamide, is connected with a transparent conductive film covering the input terminal with an anisotropic conductive adhesive. The anisotropic conductive adhesive is comprised of an adhesive 1026, and particles 127 mixed therewith and having a conductive surface with a diameter of

several tens ~ several hundreds of µm plated with gold or the like; the particles 1027 contact the transparent conductive film on the input terminal 1001 and the copper wiring 1028, thereby forming an electrical contact in this portion. Further, in order to increase mechanical strength in this part, a resin layer 1030 is provided. In this way, an active matrix liquid crystal display device as shown in Fig. 16 is completed.

[0139]

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In the active matrix liquid crystal display device, the source wiring is covered by a conductive film 1020 which is the same material as the pixel electrode, so that it has a structure that protects the entire substrate from external static electricity or the like. Alternatively, the structure, in which a protective circuit is formed in the region other than the pixel TFT portion with the conductive film 1020, may be adopted. Such a structure enables prevention of occurrence of the static electricity due to friction between the manufacturing device and the insulating substrate in the manufacturing process. In particular, the TFT or the like can be protected from the static electricity that generates at the time of rubbing in a liquid crystal orientation process performed in the manufacturing process.

[Embodiment 9]

The TFT formed by implementation of any one of Embodiments 1 to 8 described above can be used in various electro-optical devices (an active matrix type liquid crystal display and an active matrix type EC display). Namely, the invention of this specification can be implemented in all electronic equipment in which these electro-optical devices are built into a display portion.

[0140]

The following can be given as such electronic equipment: a video camera, a

digital camera, a projector (rear type or front type), a head-mounted display (goggle type display), a car navigation system, a car stereo, a personal computer, a portable information terminal (a mobile computer, a portable telephone, an electronic book, or the like), and the like. Examples of these are shown in Fig. 18 and Fig. 19.

5 [0141]

Fig. 18(A) is a personal computer, which includes a main body 2001, an image input portion 2002, a display portion 2003, a keyboard 2004, and the like. The present invention can be applied to the display portion 2003.

[0142]

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Fig. 18(B) is a video camera, which includes a main body 2101, a display portion 2102, an audio input portion 2103, operation switches 2104, a battery 2105, an image receiving portion 2106, and the like. The present invention can be applied to the display portion 2102.

[0143]

Fig. 18(C) is a mobile computer (mobile computer), which includes a main body 2201, a camera portion 2202, an image receiving portion 2203, operation switches 2204, a display portion 2205, and the like. The present invention can be applied to the display portion 2205.

[0144]

Fig. 18(D) is a goggle type display, which includes a main body 2301, a display portion 2302, an arm portion 2303, and the like. The present invention can be applied to the display portion 2302.

[0145]

Fig. 18(E) is a player that uses a recording medium on which a program is

recorded (hereafter referred to as a recording medium), which includes a main body 2401, a display portion 2402, a speaker portion 2403, a recording medium 2404, operation switches 2405, and the like. Note that this player uses a DVD (digital versatile disk), a CD, or the like as a recording medium, and music appreciation, movie appreciation, game playing and the Internet can be performed. The present invention can be applied to the display portion 2402.

[0146]

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Fig. 18(F) is a digital camera, which includes a main body 2501, a display portion 2502, an eyepiece portion 2503, operation switches 2504, an image receiving portion (not shown), and the like. The invention of this specification can be applied to the display portion 2502.

[0147]

Fig. 19(A) is a portable telephone, which includes a main body 2901, an audio output portion 2902, an audio input portion 2903, a display portion 2904, operation switches 2905, an antenna 2906, and the like. The invention of this specification can be applied to the display portion 2904.

[0148]

Fig. 19(B) is a portable book (electronic book), which includes a main body 3001, display portions 3002 and 3003, a recording medium 3004, operation switches 3005, an antenna 3006, and the like. The present invention can be applied to the display portions 3002 and 3003.

[0149]

Fig. 19(C) is a display, which includes a main body 3101, a support stand 3102, a display portion 3103, and the like. The present invention can be applied to the

display portion 3103. The display of the present invention is advantageous particularly in the case of enlarging a screen, and is advantageous for a display which has a diagonal of 10 inches or greater (especially 30 inches or greater).

[0150]

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An applicable range of the invention of this specification is thus extremely wide, and an application to electronic equipment in all fields is possible. Further, the electronic equipment of this embodiment can be realized by the use of a constitution of any combination of Embodiments $1 \sim 7$.

[0151]

10 [Effect of the Invention]

In the present invention, a light shielding portion is formed from a stacked film (R + B) formed of two colored layers. As a result, a step of forming a black matrix can be omitted.

[Brief Description of the Drawings]

- 15 [Fig. 1] A top view and cross-sectional views showing an arrangement of colored layers.
 - [Fig. 2] Cross-sectional views of colored layers.
 - [Fig. 3] A view showing a reflectivity of a stacked colored layer.
 - [Fig. 4] Views showing an overlapping of a wiring and colored layers.
- [Fig. 5] Views showing a manufacturing process of an AM-LCD.
 - [Fig. 6] Views showing a manufacturing process of an AM-LCD.
 - [Fig. 7] A top view showing a pixel.
 - [Fig. 8] A view showing a manufacturing process of an AM-LCD.
 - [Fig. 9] A top view showing a pixel.

- [Fig. 10] A cross-sectional view showing an active matrix liquid crystal display device.
- [Fig. 11] A view showing an arrangement of colored layers.
- [Fig. 12] A view showing an external view of an AM-LCD.
- [Fig. 13] Views showing a terminal portion of an AM-LCD.
- 5 [Fig. 14] A cross-sectional view showing an active matrix liquid crystal display device.
 - [Fig. 15] A cross-sectional view showing an active matrix liquid crystal display device.
 - [Fig. 16] A cross-sectional view showing an active matrix liquid crystal display device.
 - [Fig. 17] A view showing a transmittivity of a single layer of a colored layer.
 - [Fig. 18] Views showing examples of electronic equipment.
- 10 [Fig. 19] Views showing examples of electronic equipment.

[Name of Document] Abstract

[Summary]

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[Problem] In a conventional liquid crystal display device using a metallic film as a light shielding mask of a color filter, there has been a problem in that a parasitic capacitance with other wirings is formed and delay in signals tends to occur. Furthermore, in the case that an organic film containing a black pigment is used as a light shielding mask of a color filter, a problem of an increase in manufacturing steps has occurred.

[Solving Means] In the present invention, without using a light shielding mask (black matrix), a stacked film of two colored layers (a stacked film of a blue-colored layer 11 and a red-colored layer 12) is formed over an opposing substrate as a light shielding portion 15 so as to overlap with a TFT and a source wiring on an element substrate.

[Selected Drawing] Fig. 1